Figure 1a

Figure 1b

Figure 2a (prior art)

input u_k

$x_{k,1} = u_k$

$x_{k,2}$

D   D   D

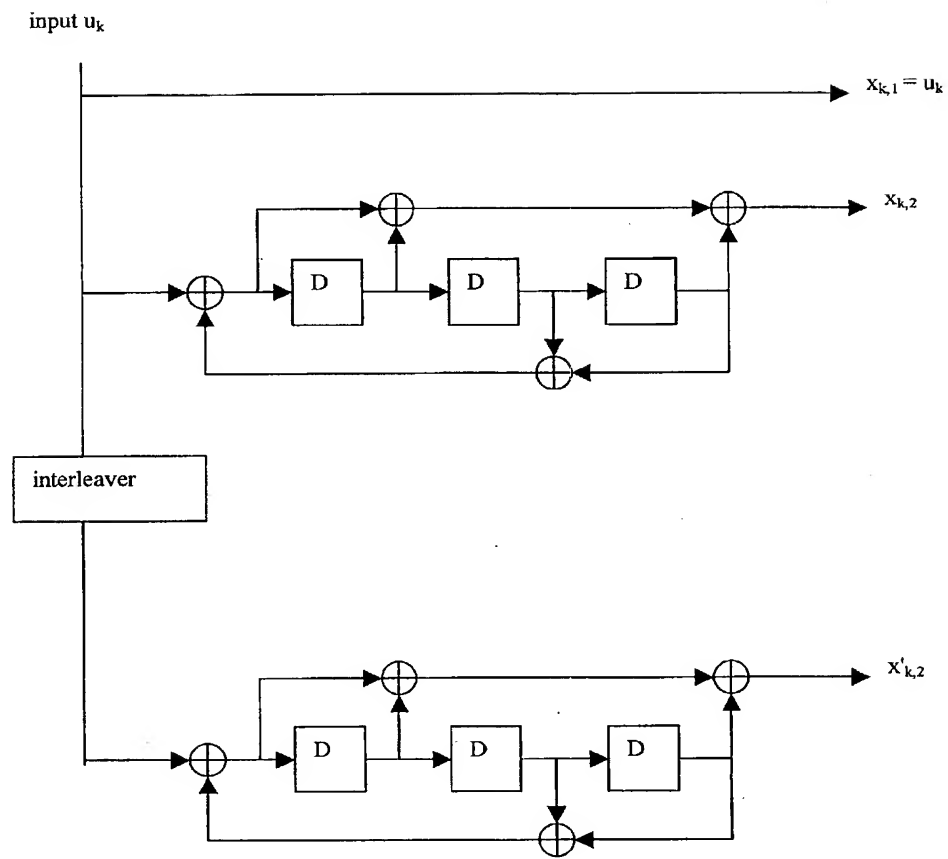interleaver

$x'_{k,2}$

D   D   D

Figure 2b (prior art)

extrinsic info

interleaved extrinsic info

$y_{k,2}$ → MAP decoder → interleaver → MAP decoder → deinterleaver

$y_{k,1}$ →

interleaver

$y'_{k,2}$ →

extrinsic info

$y_{k,1}$

hard decision

u_k estimate

Figure 2c (prior art)

Beta State Metrics

Beta
Block

Beta
RAM

Extrinsics
Block

Alpha
Block

Extrinsics

Alpha State Metrics
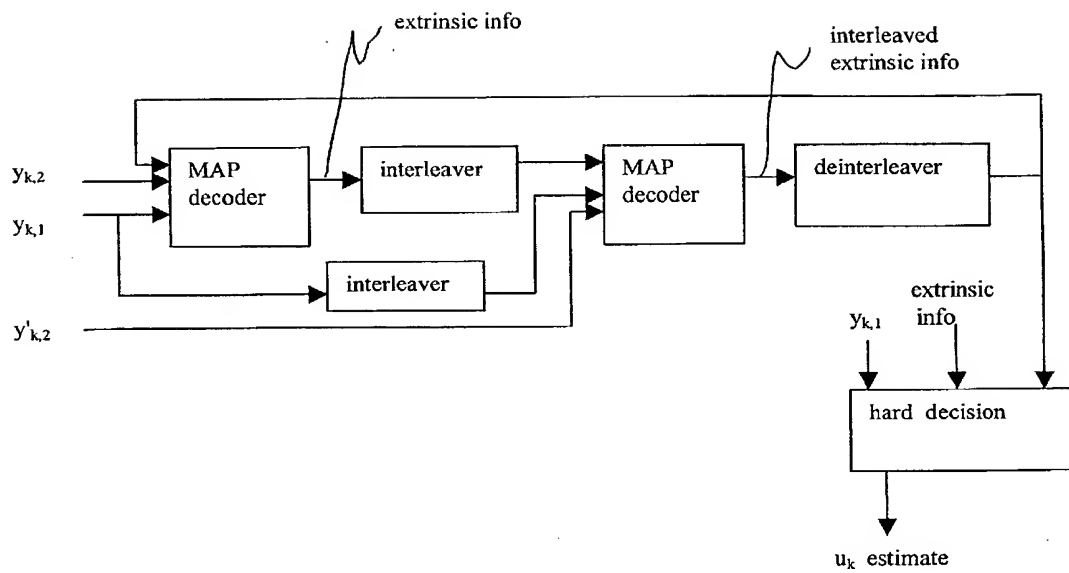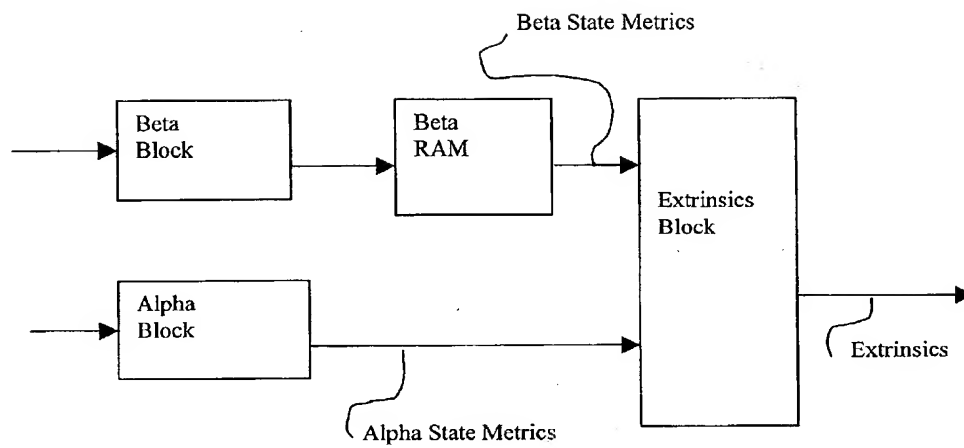
Figure 2d beta block (prior art)

Beta

$L_c\, y_{1,k}$

$L_c\, y_{2,k}$

a priori

adder tree

max*

max*

max*

max* registers

normalization

registers

write to
Beta
RAM

Figure 2e   alpha block

Labels in figure:
- adder tree
- max*
- max*
- max*
- max* registers
- normalization
- registers
- Alpha
- $L_c\, y_{1,k}$
- $L_c\, y_{2,k}$
- a priori
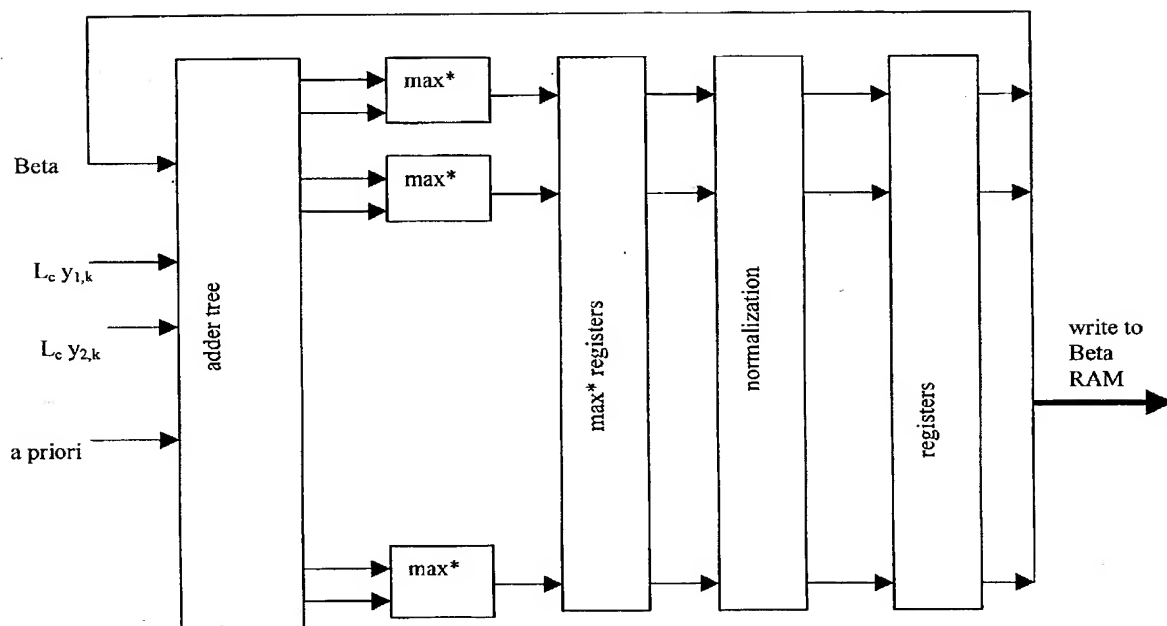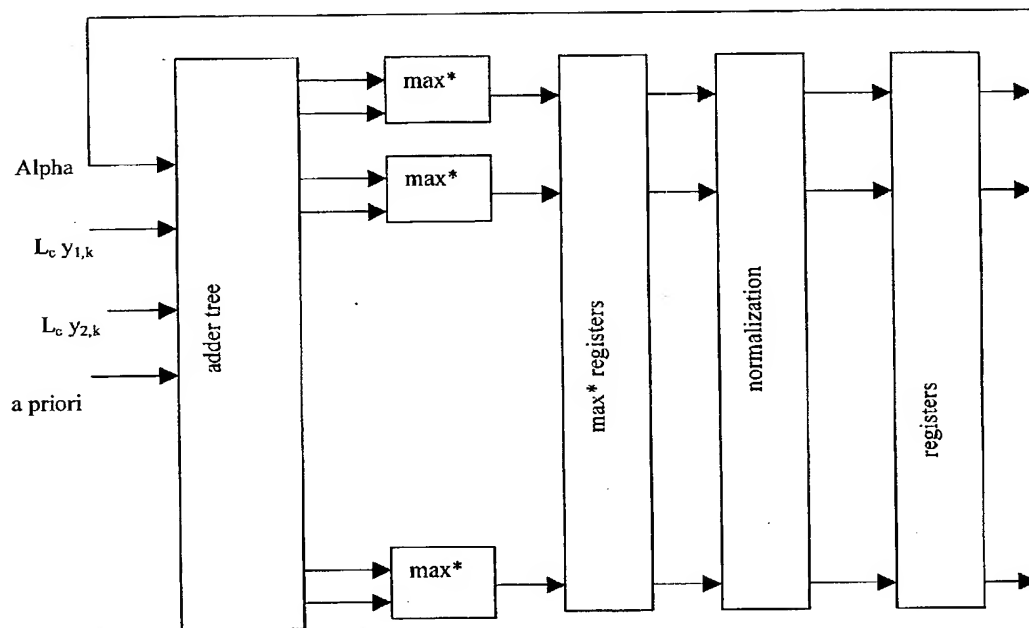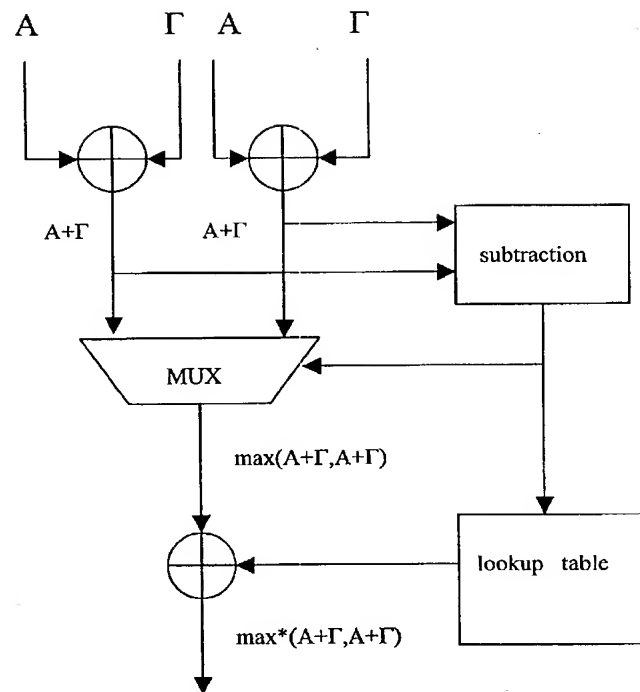
Figure 2f   extrinsic block (prior art)
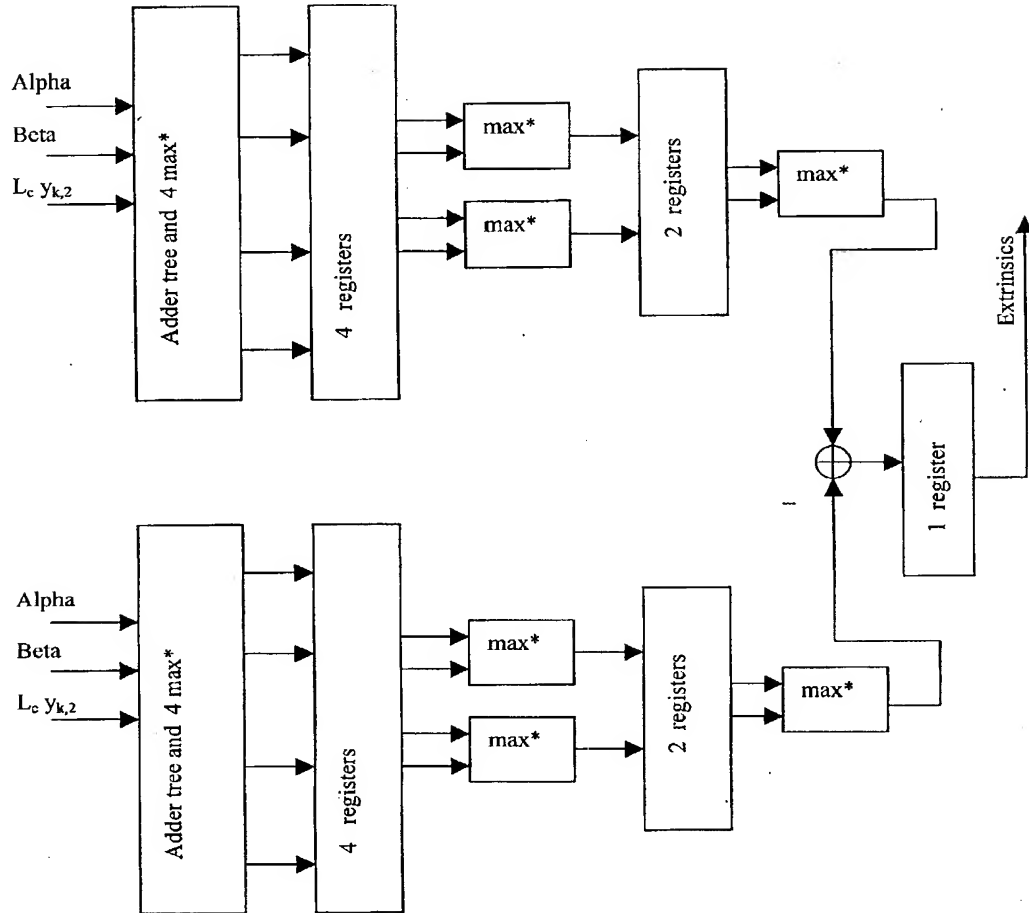
Figure 2g adder plus max* circuit (prior art)

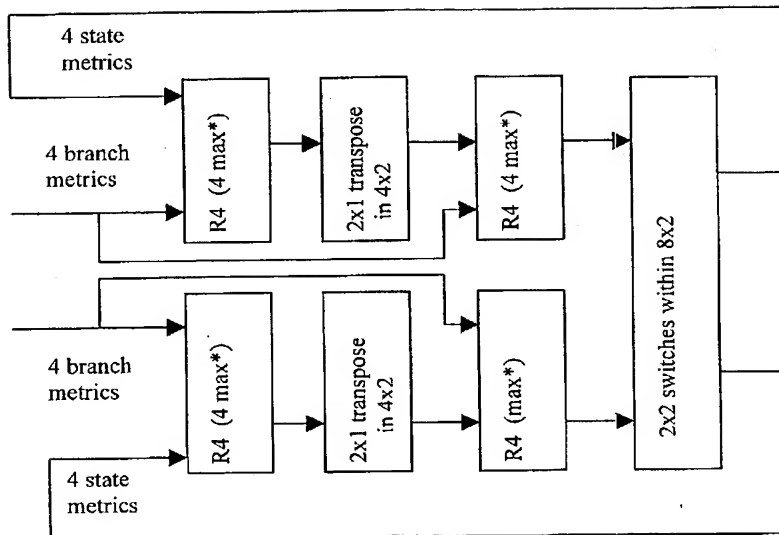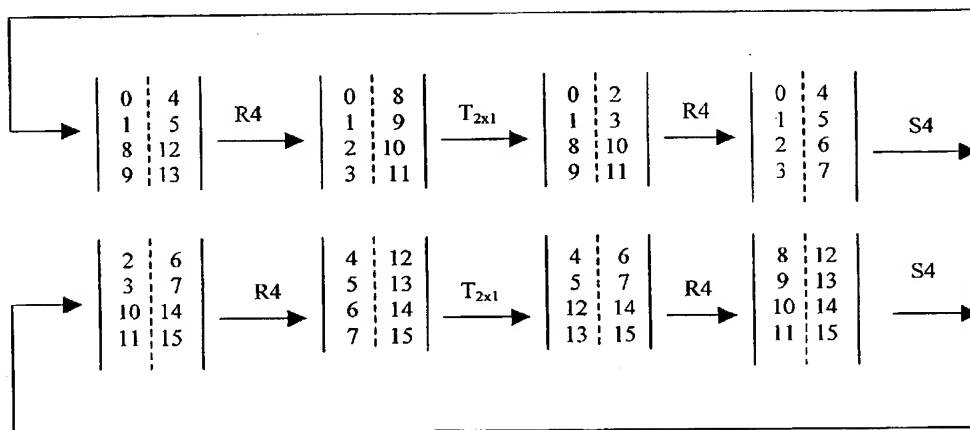# Figure 3a alpha block

Figure 3b

Figure 3c first architecture beta block

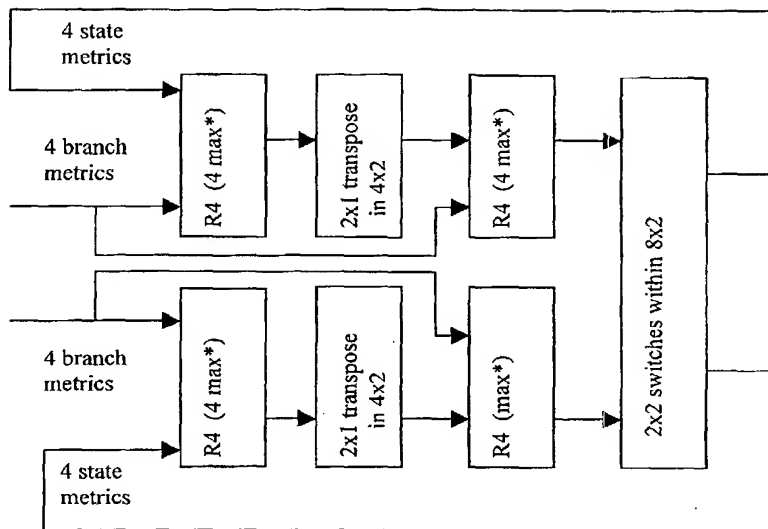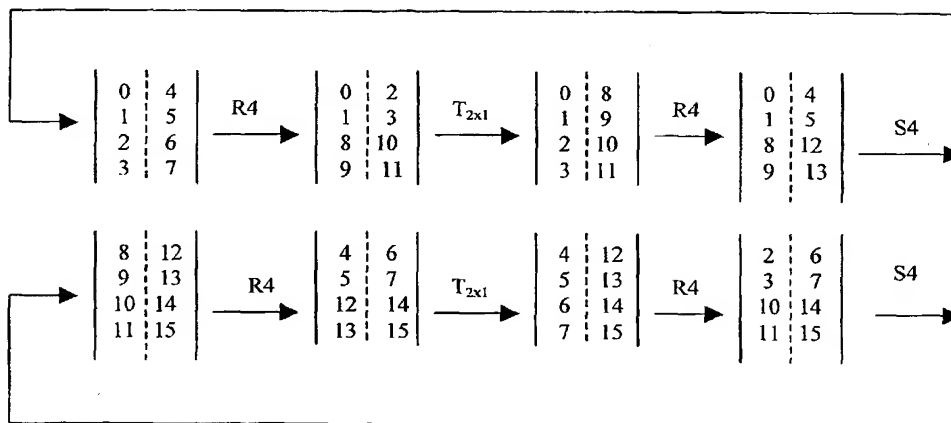## Figure 3d
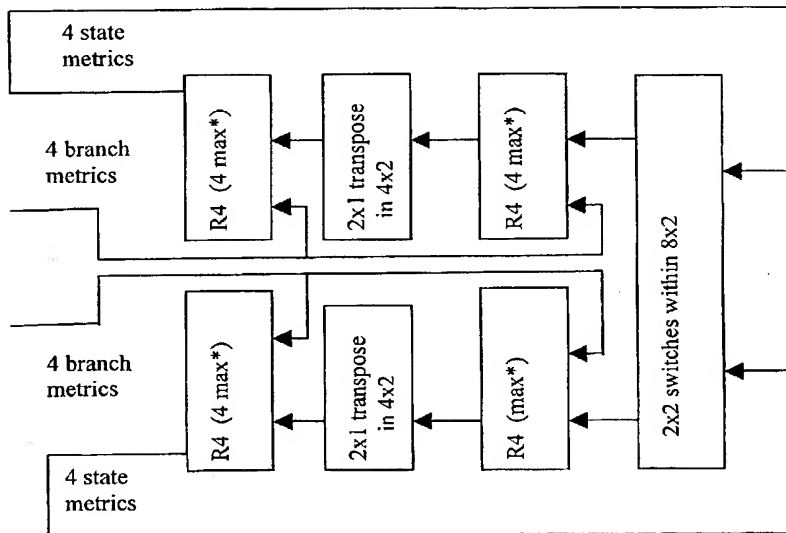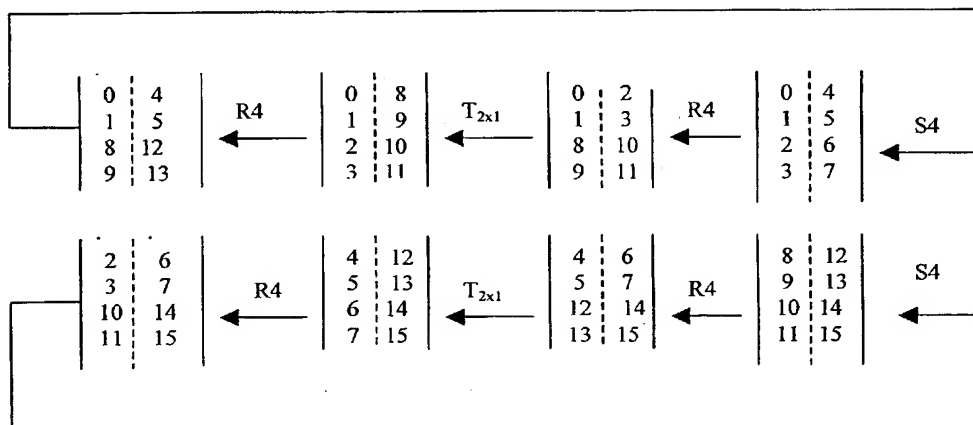
Figure 3e second architecture beta block

4 state metrics

4 branch metrics

R4 (4 max*)

2x1 transpose in 4x2

R4 (4 max*)

2x2 switches within 8x2

4 branch metrics

R4 (4 max*)

2x1 transpose in 4x2

R4 (max*)

4 state metrics

Figure 3f

0	4		0	8		0	2		0	4	
1	5	R4	1	9	T$_{2x1}$	1	3	R4	1	5	S4
8	12		2	10		8	10		2	6	
9	13		3	11		9	11		3	7	

2	6		4	12		4	6		8	12	
3	7	R4	5	13	T$_{2x1}$	5	7	R4	9	13	S4
10	14		6	14		12	14		10	14	
11	15		7	15		13	15		11	15	

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Figure 3g cascade extrinsic subblock

$$\log[\ \textstyle\sum_{\text{states}} \exp(A_{k-1} + \Gamma_k + B_k)\ ]$$
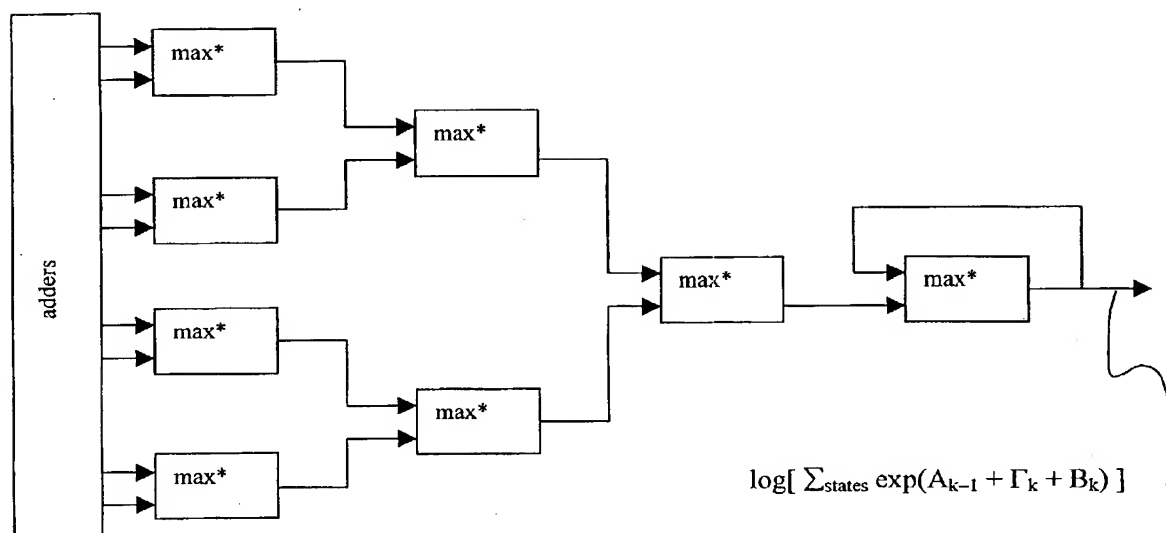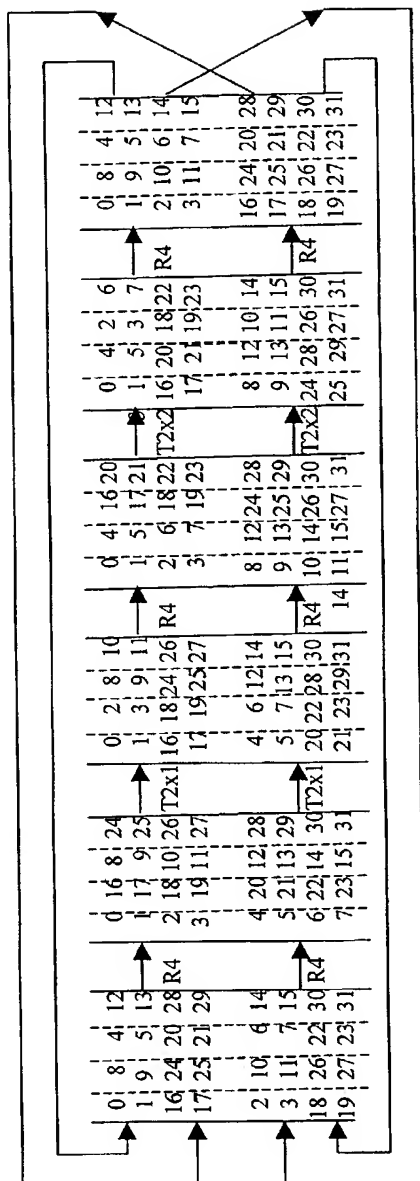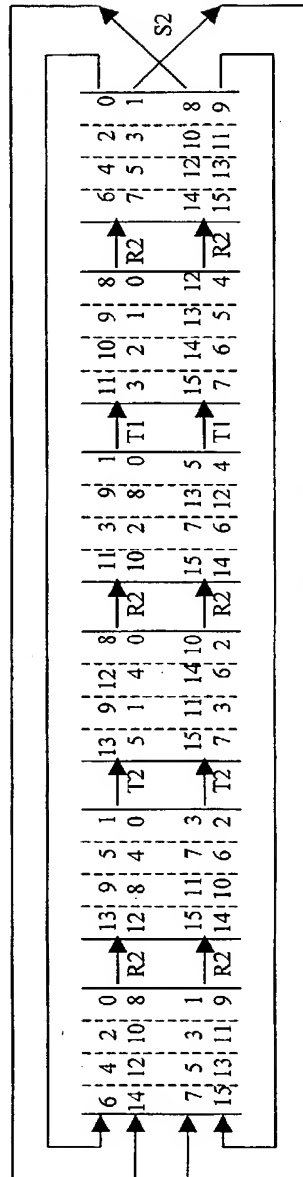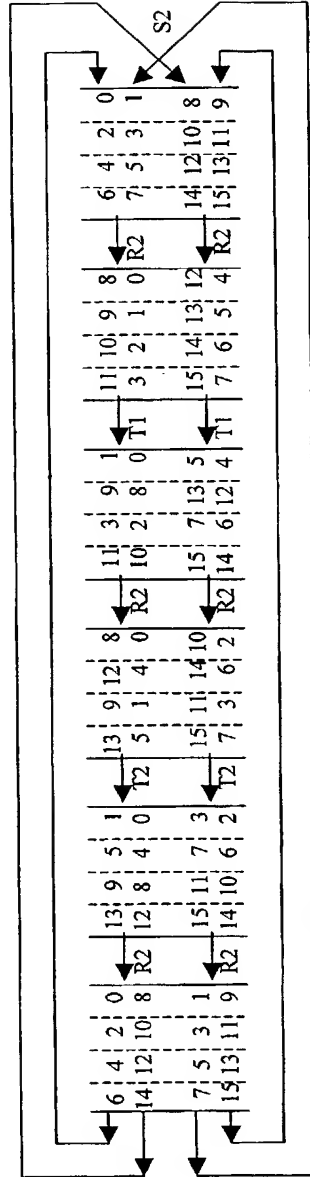
Figure 4 alpha block

Figure 5a alpha block

Figure 5b beta block

Figure 5c extrinsics block